

Model Name: GA-H81M-H

Revision 2.1

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1150-A
05	CPU_LGA1150-B
06	CPU_LGA1150-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESS X1 *2 SLOT
16	ITE 8620
17	COM,KB_MS_USB,USB30_20
18	HWM,FAN CTRL,OV,-PROCHOT
19	DUAL BIOS
20	FP,FUSB,SPK,SATALED
21	Realtek ALC887-VD2
22	REAR AUDIO JACK
23	REALTEK RTL8111G
24	DISCRETE POWER
25	ATX , CLOCK GEN
26	VCORE ISL95812_1
27	VCORE ISL95812_2

SHEET

TITLE

28	RT8120_DDR POWER
29	HDMI
30	
31	
32	

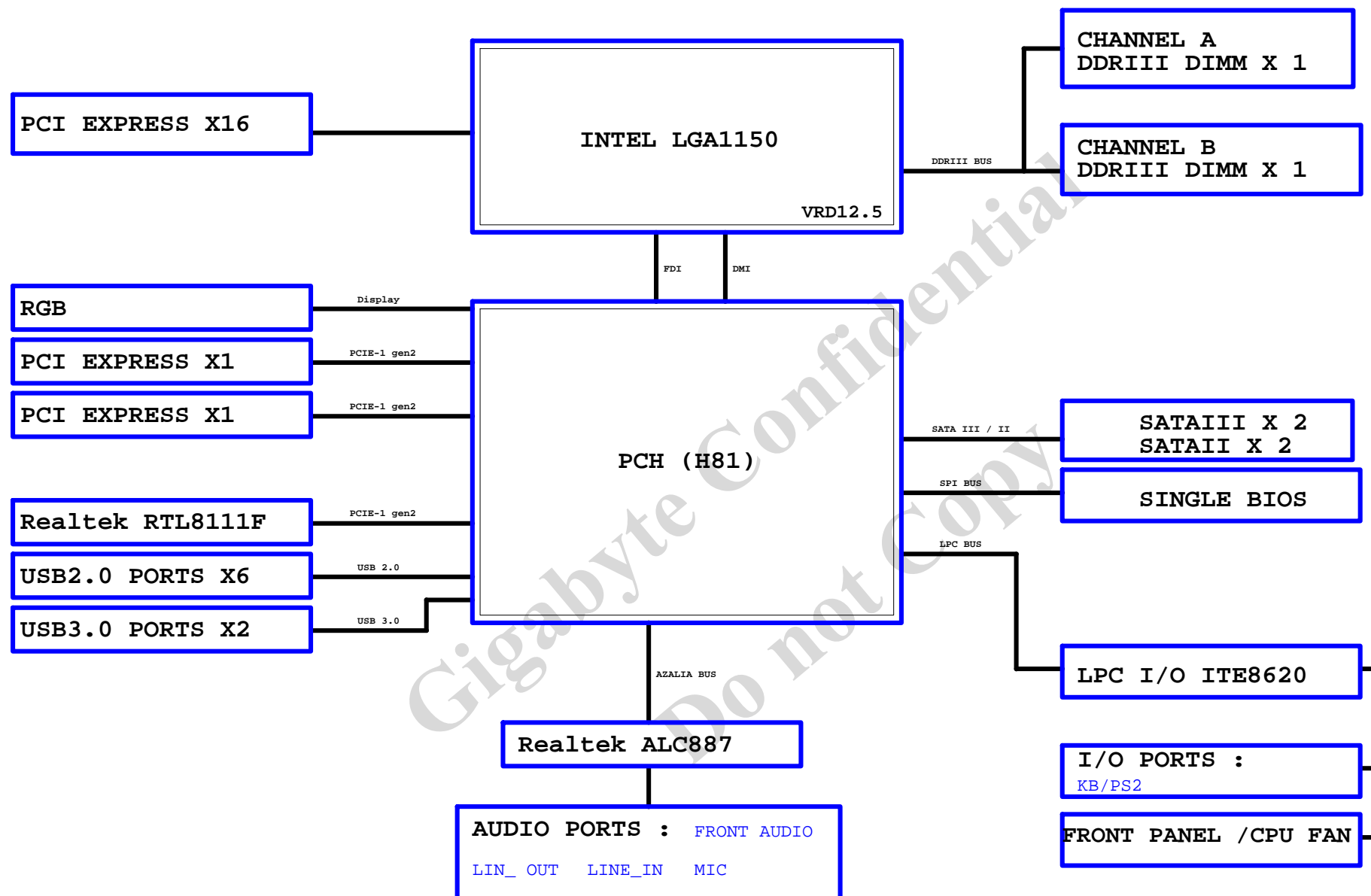
Gigabyte Technology

Cover Sheet

Size Custom	Document Number GA-H81M-H	Rev 2.1
Date:	Thursday, November 20, 2014	Sheet 1 of 29

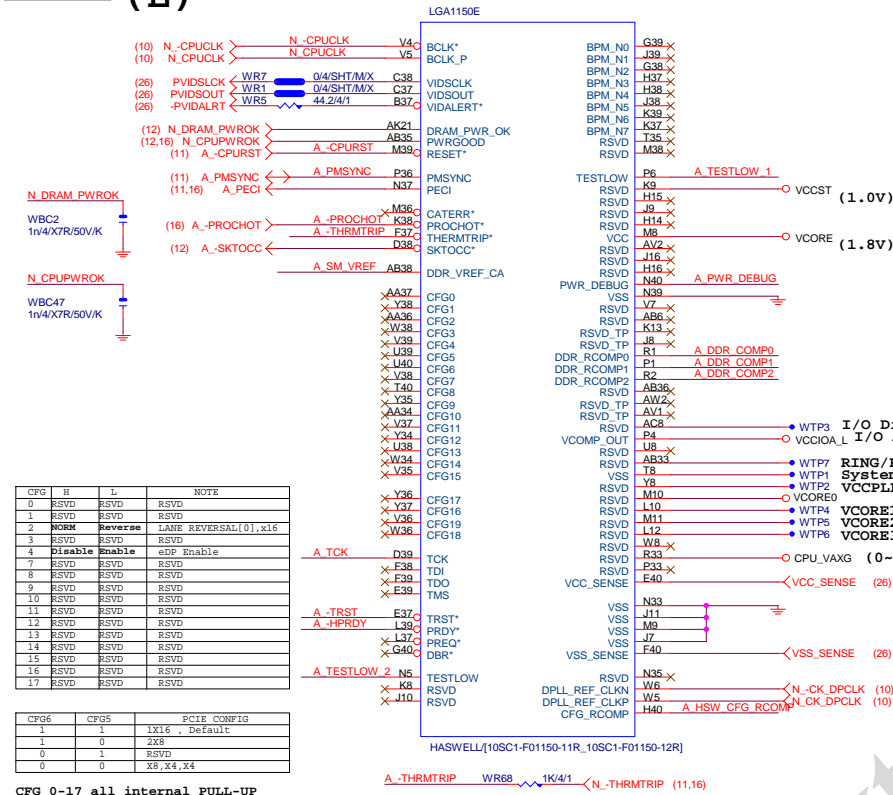
[illegible][illegible][illegible][illegible][illegible][illegible]

BLOCK DIAGRAM



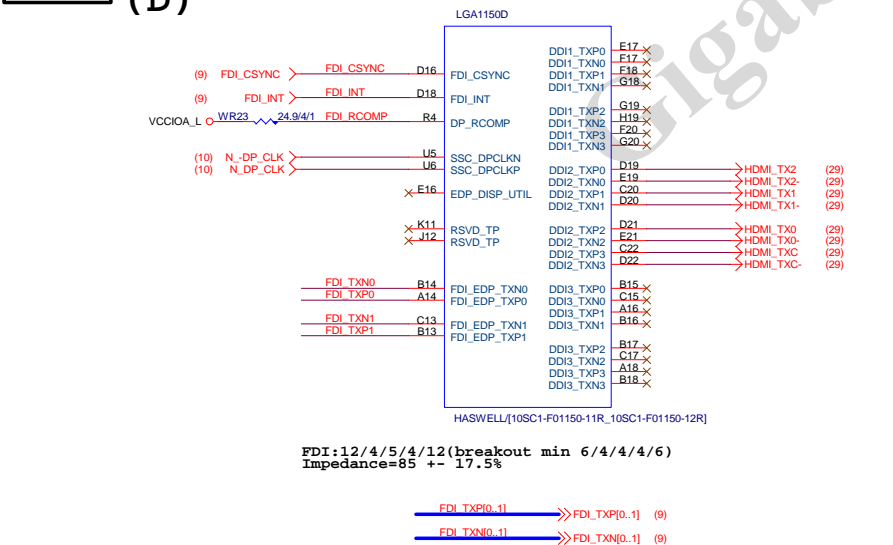
LGA1150

(E)



LGA1150

(D)

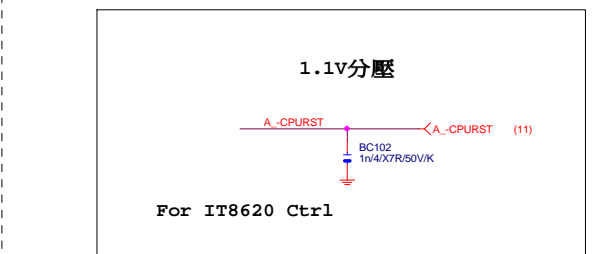


LGA1155

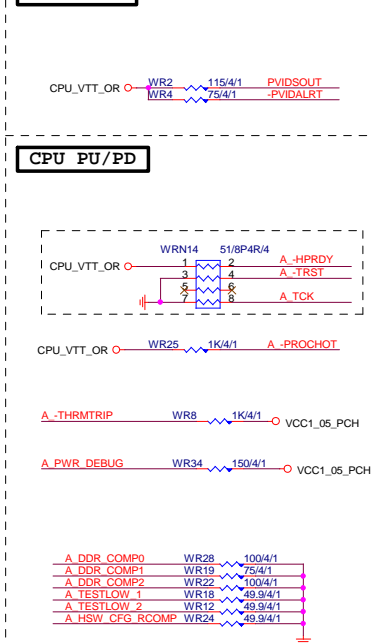
(C)



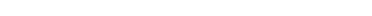
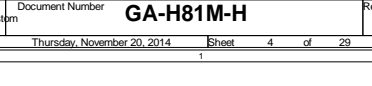
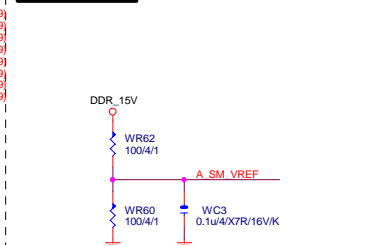
-CPURST

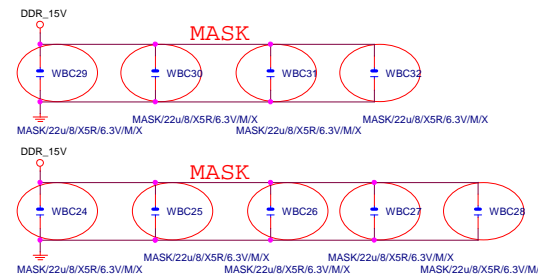
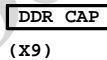
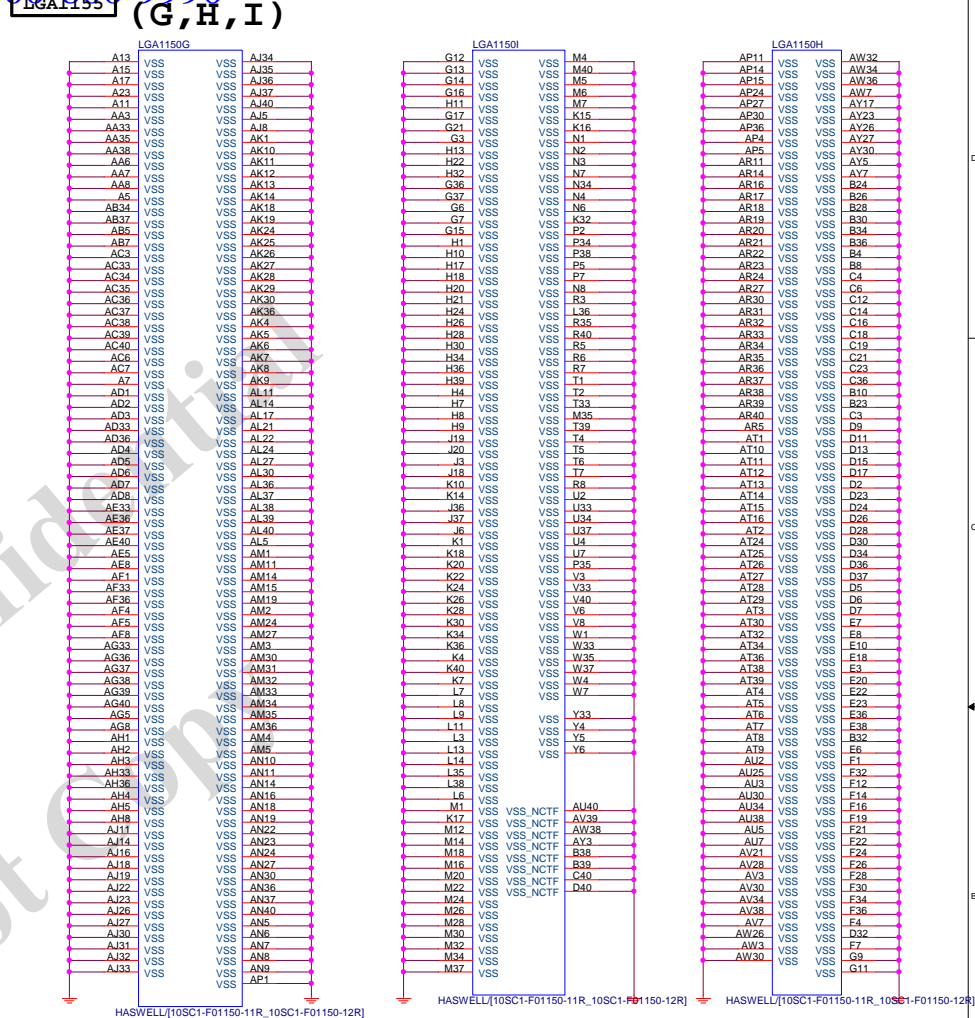


CPU SVID

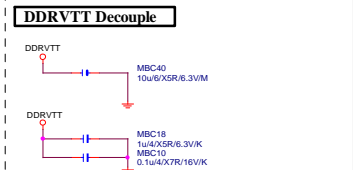
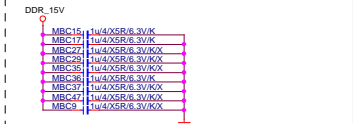


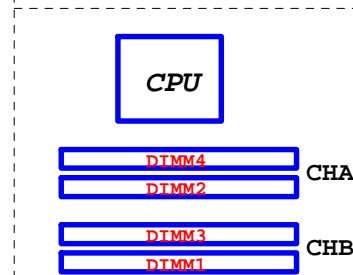
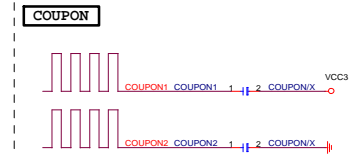
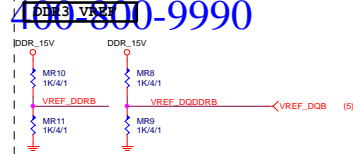
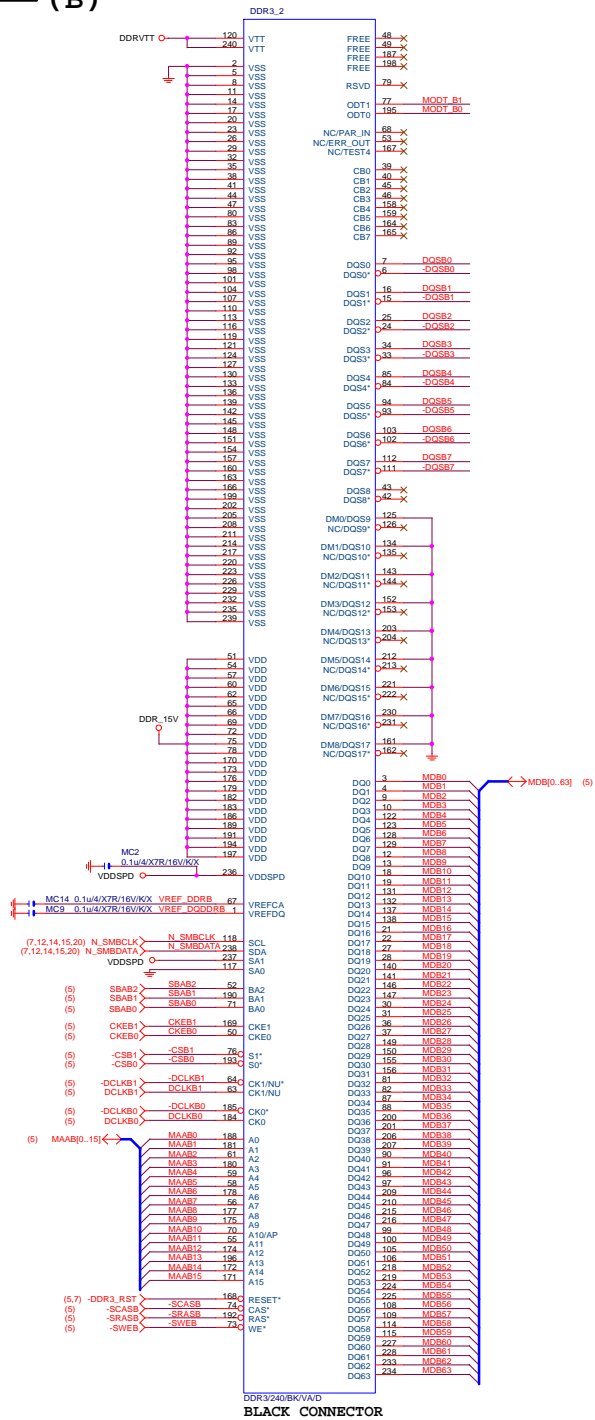
SM REF



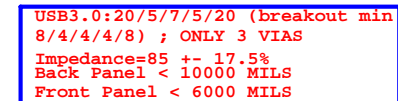


DDR3





PCHF



PCIEx1

N/A

```

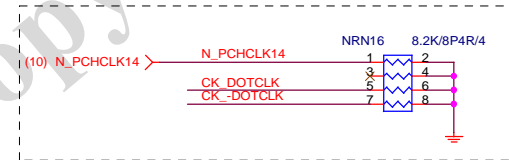
_PCIEX1:16/5/5/5/16 (breakout min 8/4/4/4/8)

```

PCH H/S

PCH CLK PD

Mount for integrated clock Generation Mode



USB TABLE

```
OC[3:0]# for Device 29 (ports 0-7)
OC[7:4]# for Device 26 (ports 8-13)
```

USB OC#	Configure
OC0#	R_USB30
OC1#	USB_LAN
OC2#	Not Use
OC3#	N/A
OC4#	F_USB1
OC5#	F_USB2
OC6#	Not Use
OC7#	N/A

Gigabyte Technology

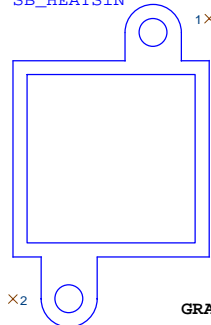
Title	PCH FDI,DMI,USB ,PCIE,NVRAM
-------	-----------------------------

Size Custom	Document Number GA-H81M-H	Rev 2.1
----------------	-------------------------------------	------------

Date:	Thursday, November 20, 2014	Sheet	9	of	29
-------	-----------------------------	-------	---	----	----

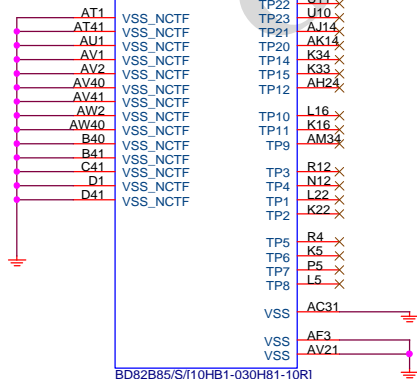
LOW COST ICH7 HEATSINK

SB_HEATSIN

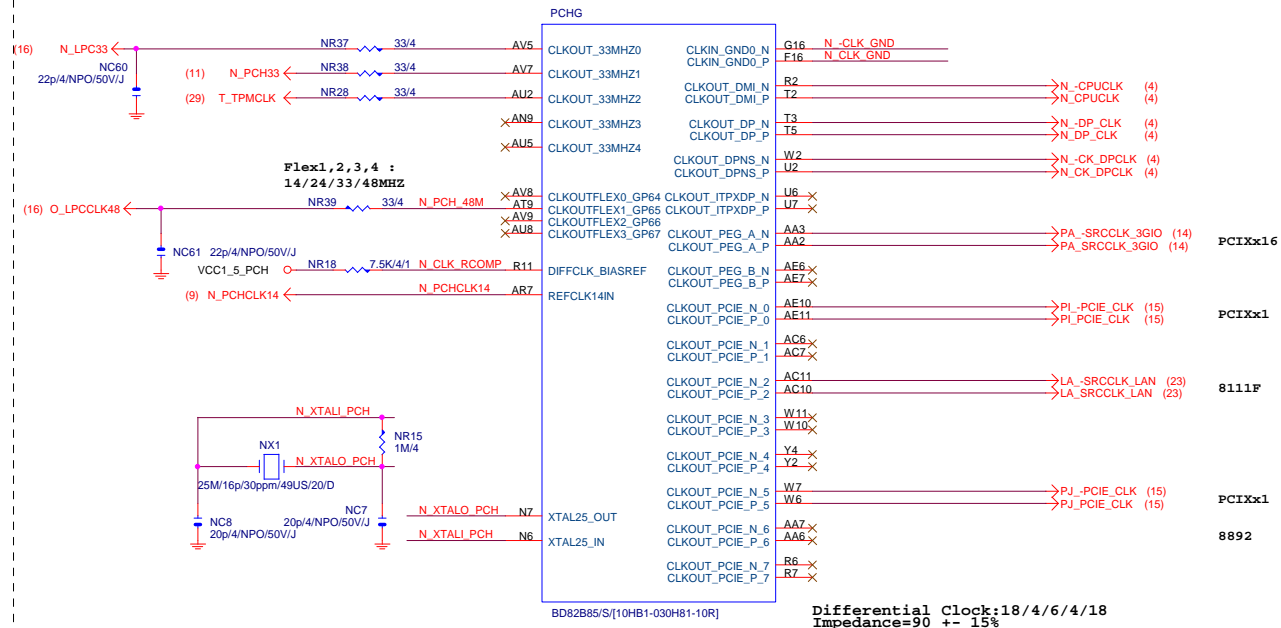
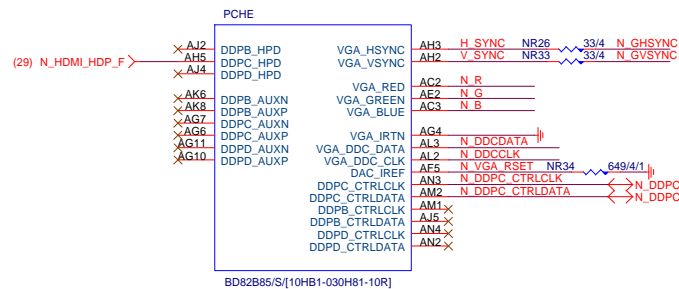


PCH_HS
PCH_HS/12SP2-030005-43R_12SP2-030005-41R_12SP2-030005-42R

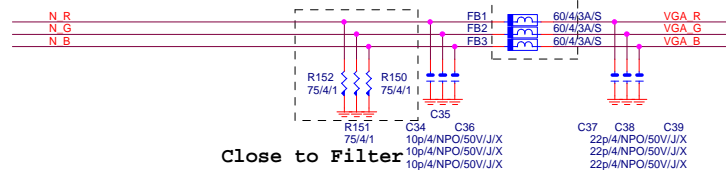
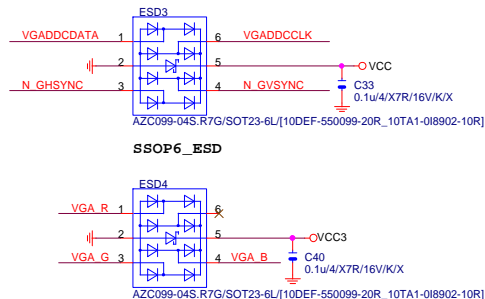
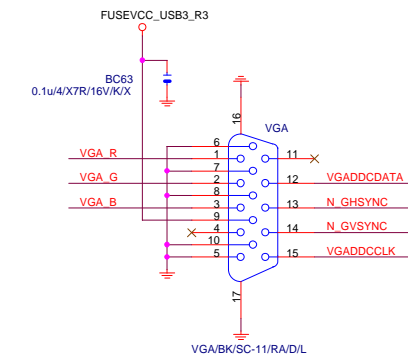
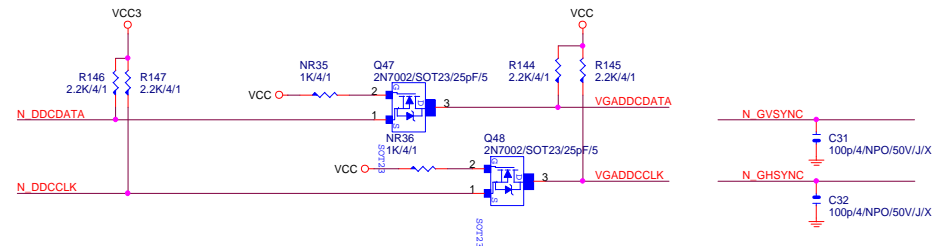
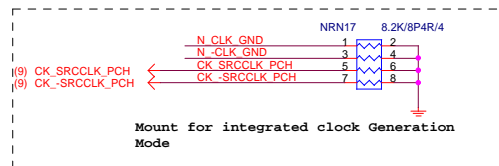
PCHJ



BD82B85/S/10HB1-030H81-10R



Differential Clock:18/4/6/4/18
Impedance=90 +- 15%



Gigabyte Technology

PCH DISPLAY ,CLK BUFFER

GA-H81M-H

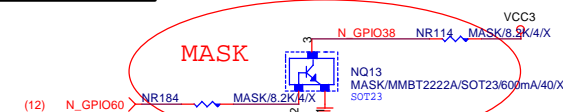
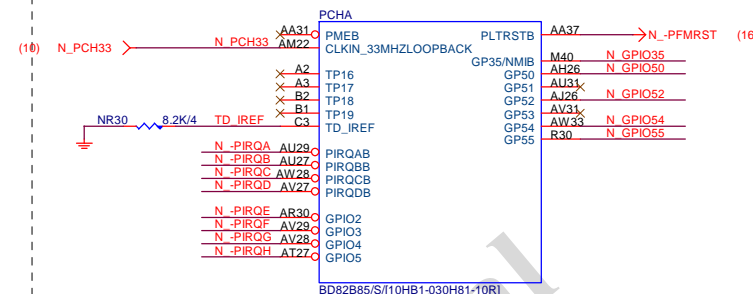
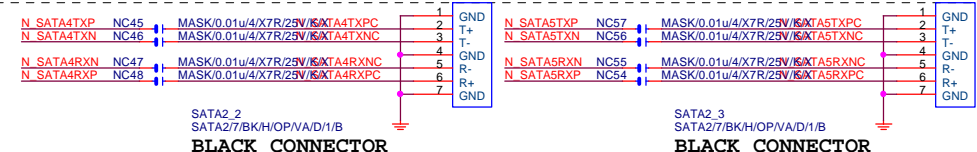
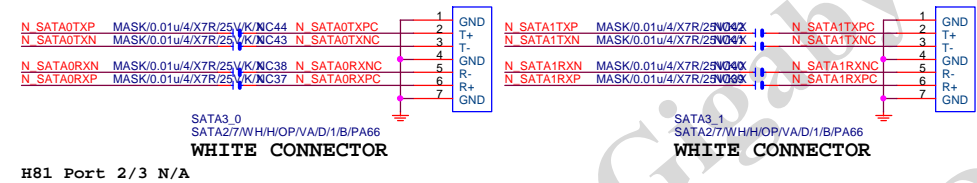
2.4

Figure 1 shows the pin connections for the NXP LPC1114. The diagram illustrates three 8-pin connectors: NR2, NR3, and NR7. Each connector has pins 1 through 8. Pin 1 is labeled N -PIRQC, N -PIROH, N -PIROD, and N -PIROB. Pin 2 is labeled 8.2K/8P4R/4. Pin 3 is labeled N -PIROE, N -PIROF, N -PIROA, and N -PIROG. Pin 4 is labeled 8.2K/8P4R/4. Pin 5 is labeled 8.2K/8P4R/4. Pin 6 is labeled 8.2K/8P4R/4. Pin 7 is labeled 8.2K/8P4R/4. Pin 8 is labeled 8.2K/8P4R/4. The VCC3 pin is connected to pin 2 of NR2, pin 4 of NR3, and pin 8 of NR7.

Timing diagram for DMI RX TERMINATION. The diagram shows signals N_GPIO48, N_GPIO35, N_GPIO16, N_SERIRQ, N_GPIO38, N_GPIO19, N_GPIO22, N_GPIO49, N_PCL_STOP, N_A20G39, N_GPIO55, N_GPIO21, N_KBRST, and N_GPIO55 connected to a 4-bit bus (pins 1, 2, 3, 4). The bus is terminated at VCC3 (8.2K/8P4R/4) and has a 1K/8P4R/4 termination resistor. The signals are shown as digital pulses. N_GPIO48, N_GPIO35, N_GPIO16, N_SERIRQ, N_GPIO38, N_GPIO19, N_GPIO22, N_GPIO49, N_PCL_STOP, N_A20G39, N_GPIO55, N_GPIO21, N_KBRST, and N_GPIO55 are all shown as active-low signals (indicated by a bubble on the input symbol).

GPIO38 Ctrl

```
** Z87/H87 Port 4&5 SATA3.0
** B85 Port 4&5 SATA2.0
```

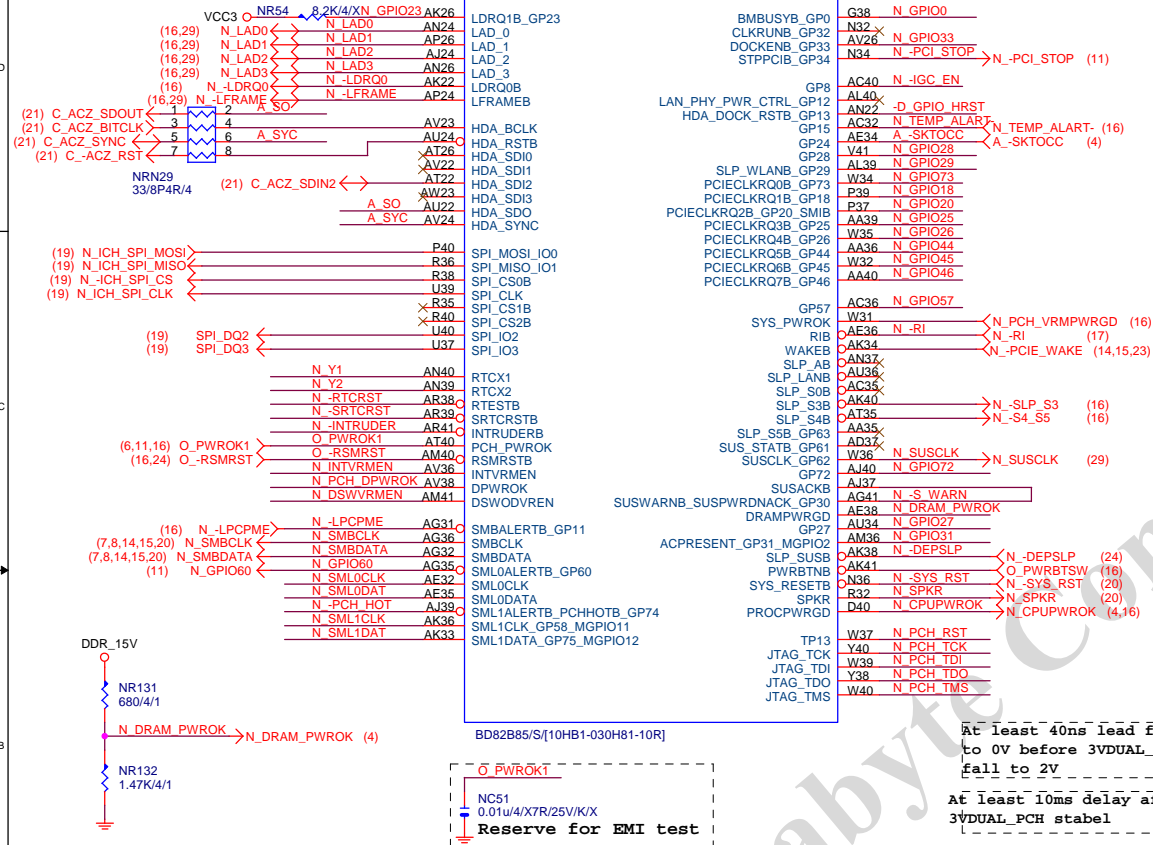


PCH

(D)

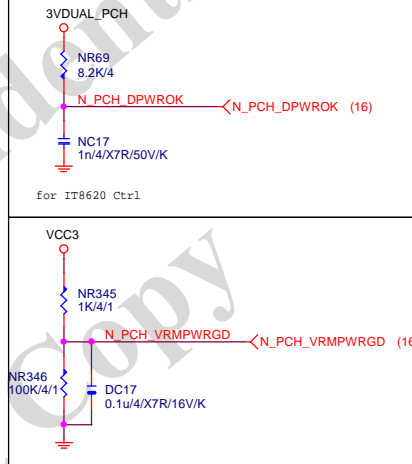
(16,29) N_LAD[0..3] <-- N_LAD[0..3]

PCHD



ACZ_SDOUT

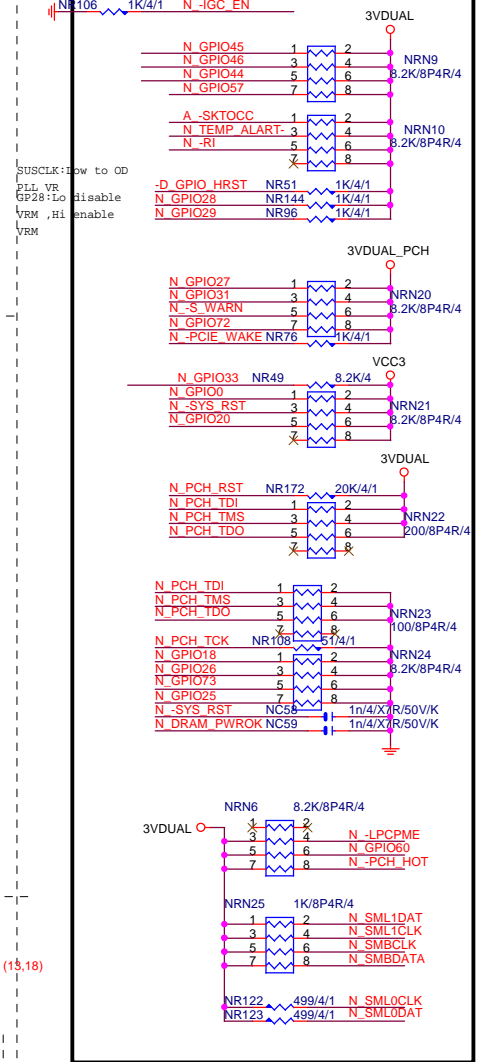
PCH_DPWROK



PCH PU/PD

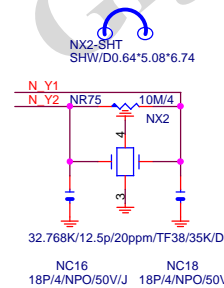
GP8: Low to enable

PCH Lock chip

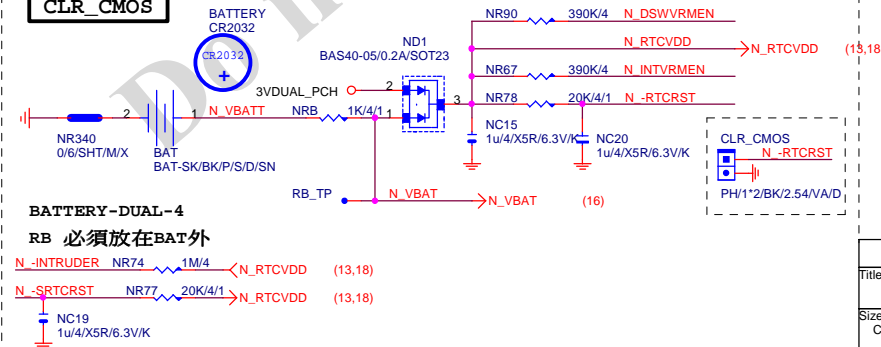


HSW_STRAP13

32.768KHZ

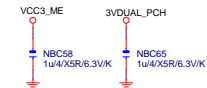


CLR_CMOS

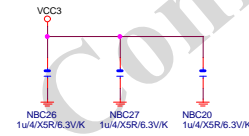


Gigabyte Technology

Title		PCH GPIO , CTRL , AUDIO	
Size	Document Number	GA-H81M-H	
Custom		Rev 2.1	
Date:	Thursday, November 20, 2014	Sheet 12	of 29



(1.05V) (x5)

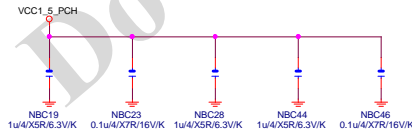


Remove

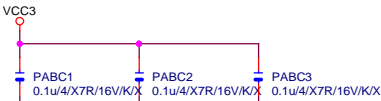
$(1.05V)(x2) + (3.3V)(x2)$



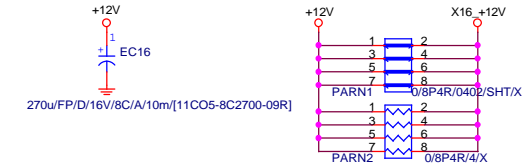
Remove

[illegible]

PCIEX16 CAP



PCIEX16 PROTECT SHT

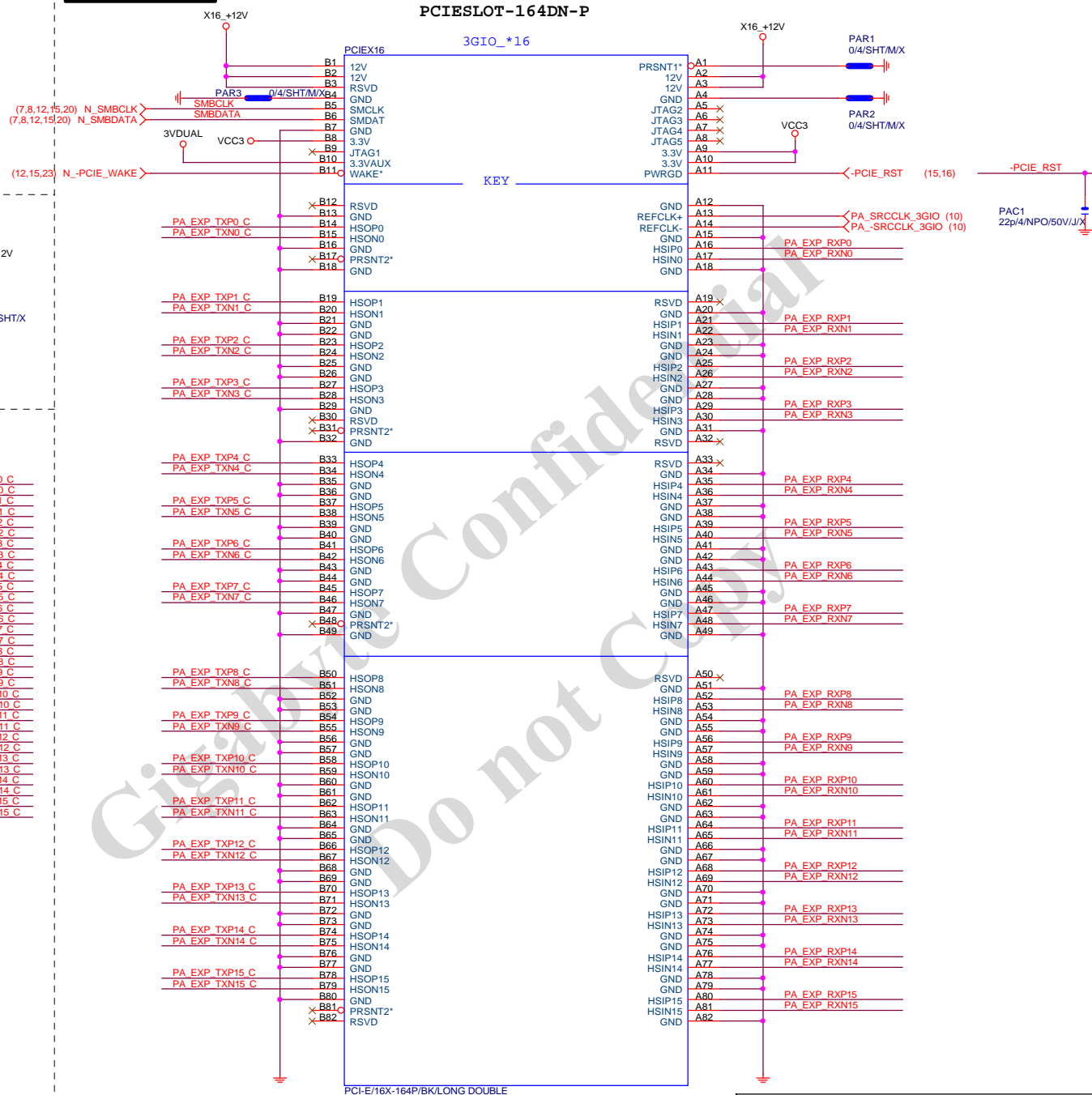


PCIEX16 AC CAP

PA EXP TXP0	PAC5	0.22u4/X5R/6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u4/X5R/6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u4/X5R/6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u4/X5R/6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u4/X5R/6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u4/X5R/6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u4/X5R/6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u4/X5R/6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u4/X5R/6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u4/X5R/6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u4/X5R/6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u4/X5R/6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u4/X5R/6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u4/X5R/6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC19	0.22u4/X5R/6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC18	0.22u4/X5R/6.3V/K	PA EXP TXN7 C
PA EXP TXP8	PAC20	0.22u4/X5R/6.3V/K	PA EXP TXP8 C
PA EXP TXN8	PAC21	0.22u4/X5R/6.3V/K	PA EXP TXN8 C
PA EXP TXP9	PAC22	0.22u4/X5R/6.3V/K	PA EXP TXP9 C
PA EXP TXN9	PAC23	0.22u4/X5R/6.3V/K	PA EXP TXN9 C
PA EXP TXP10	PAC24	0.22u4/X5R/6.3V/K	PA EXP TXP10 C
PA EXP TXN10	PAC25	0.22u4/X5R/6.3V/K	PA EXP TXN10 C
PA EXP TXP11	PAC26	0.22u4/X5R/6.3V/K	PA EXP TXP11 C
PA EXP TXN11	PAC27	0.22u4/X5R/6.3V/K	PA EXP TXN11 C
PA EXP TXP12	PAC28	0.22u4/X5R/6.3V/K	PA EXP TXP12 C
PA EXP TXN12	PAC29	0.22u4/X5R/6.3V/K	PA EXP TXN12 C
PA EXP TXP13	PAC30	0.22u4/X5R/6.3V/K	PA EXP TXP13 C
PA EXP TXN13	PAC31	0.22u4/X5R/6.3V/K	PA EXP TXN13 C
PA EXP TXP14	PAC32	0.22u4/X5R/6.3V/K	PA EXP TXP14 C
PA EXP TXN14	PAC33	0.22u4/X5R/6.3V/K	PA EXP TXN14 C
PA EXP TXP15	PAC34	0.22u4/X5R/6.3V/K	PA EXP TXP15 C
PA EXP TXN15	PAC35	0.22u4/X5R/6.3V/K	PA EXP TXN15 C

PA EXP RXIP0.15] >> PA_EXP_RXP[0.15] (4)
PA EXP RXN0.15] >> PA_EXP_RXN[0.15] (4)
PA EXP TXIP0.15] >> PA_EXP_TXP[0.15] (4)
PA EXP TXN0.15] >> PA_EXP_TXN[0.15] (4)

PCIEX16 SLOT



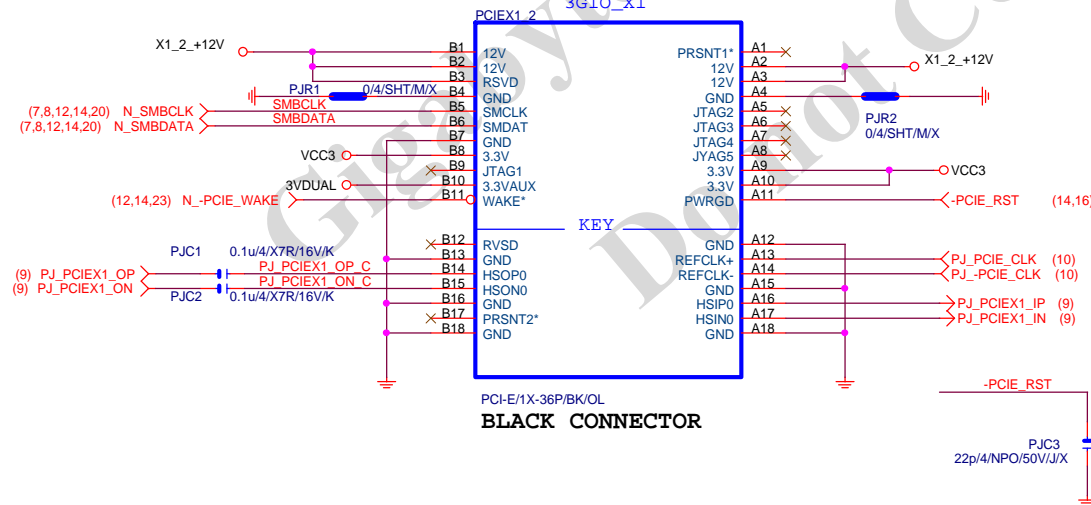
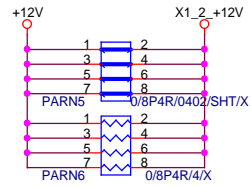
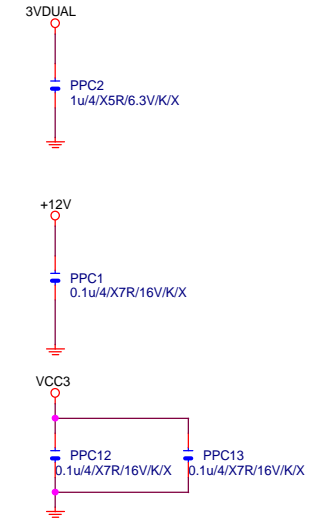
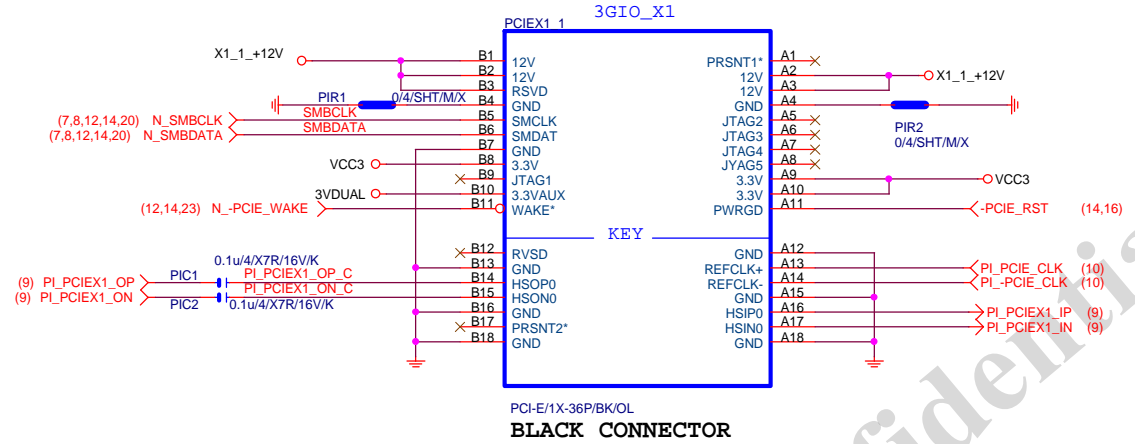
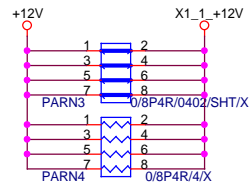
BLACK CONNECTOR

Gigabyte Technology

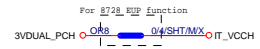
Title			PCI EXPRESS * 16		
Size			GA-H81M-H		
Custom			Rev 2.1		
Date: Thursday, November 20, 2014			Sheet 14 of 29		

PCIEX1 SLOT

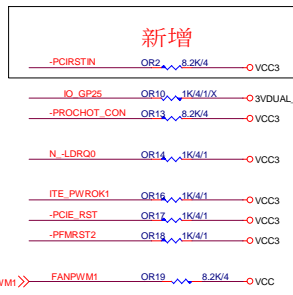
PCIEX1 PROTECT SHT



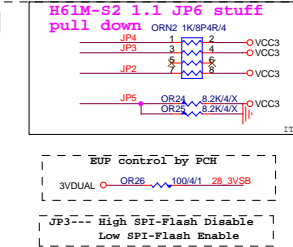
Gigabyte Technology			
PCI EXPRESS X 1 PORT			
Title	Document Number	Rev	
Size	Custom	GA-H81M-H	
Date:	Thursday, November 20, 2014	Sheet	15 of 29



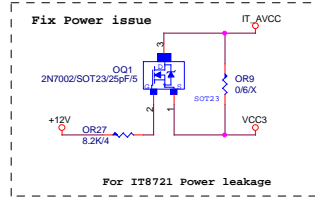
SIO PU



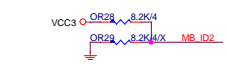
SIO STRAP



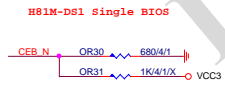
Power leakage



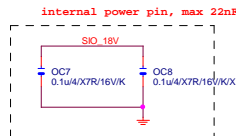
MB ID



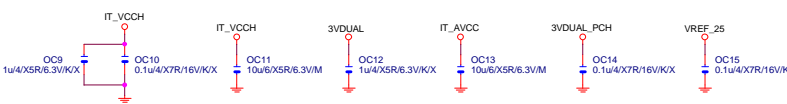
DUAL BIOS OPT STRAP



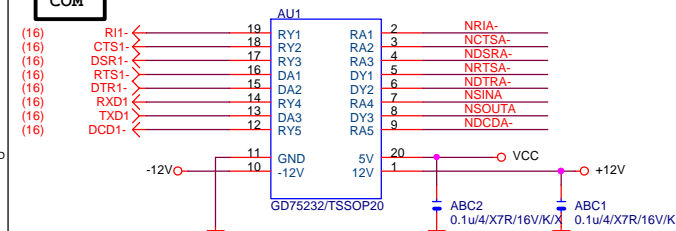
SIO 18V



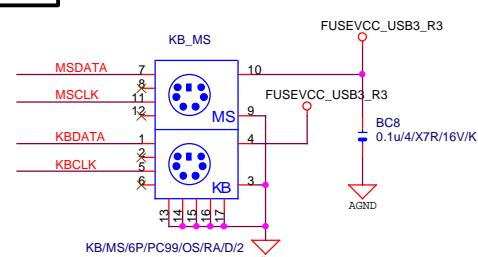
SIO CAP



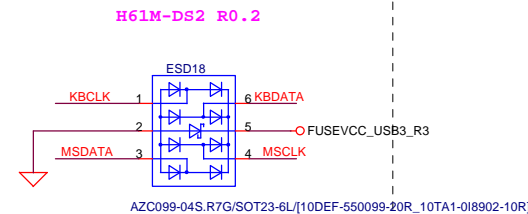
COM



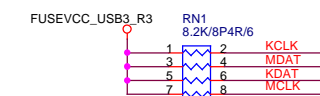
KB/MS



KB_MS ESD



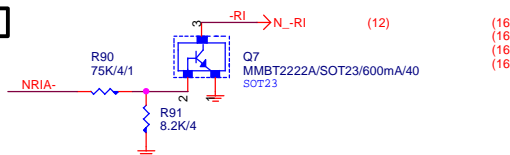
For EMI



FOR鹽化短路



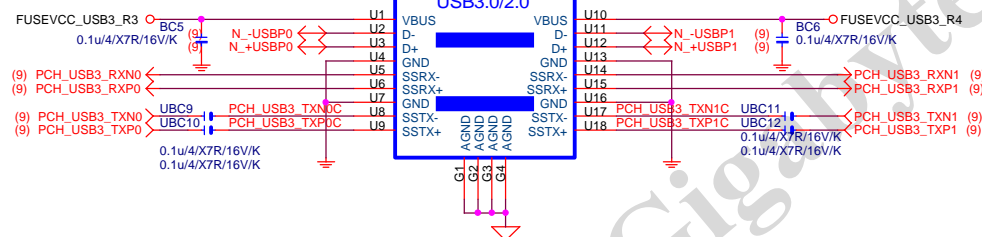
COM RI



USB30_20

R_USB30
USB/18P/BU/OS/RA/D/2/1U/USB

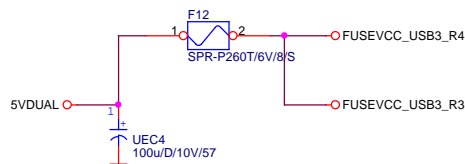
USB3.0/2.0



USB30_20 PWR

-USBOC_R

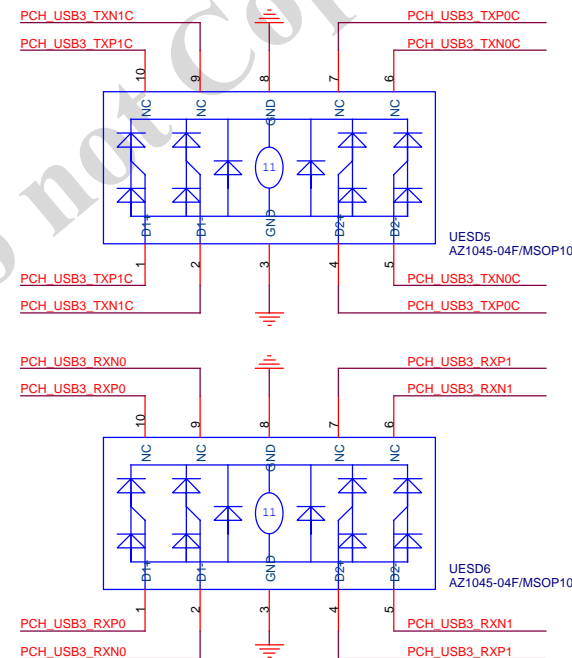
Polyswitch-1206



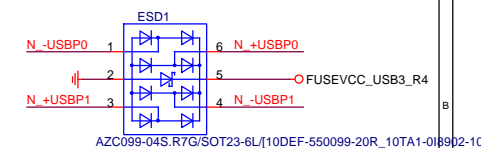
USB3.0 1Port - 1Fuse (3.5A)

USB30_20 ESD PROTECT

USB3.0 ESD



USB POWER PROTECT

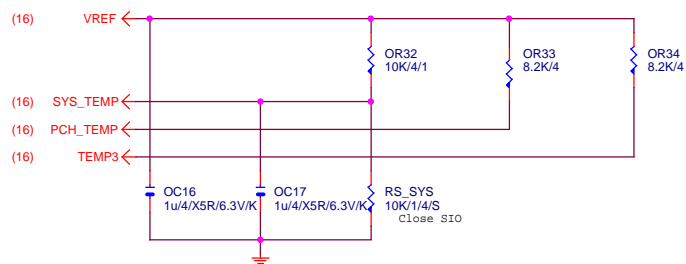


Gigabyte Technology

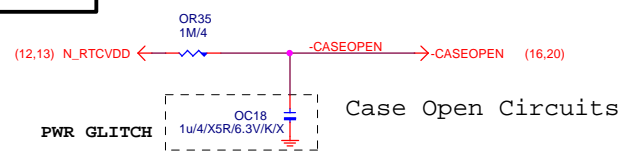
Title
COM,-RI,KB_USB,USB_ESATA,-PROCHOTSize
Custom Document Number
GA-H81M-HRev
2.1

Date: Thursday, November 20, 2014 Sheet 17 of 29

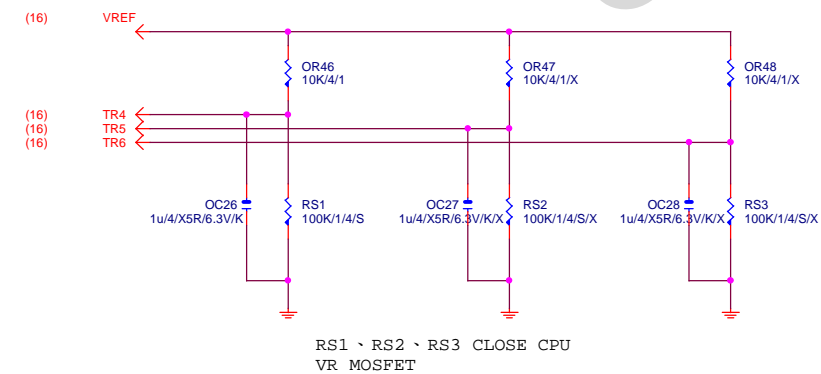
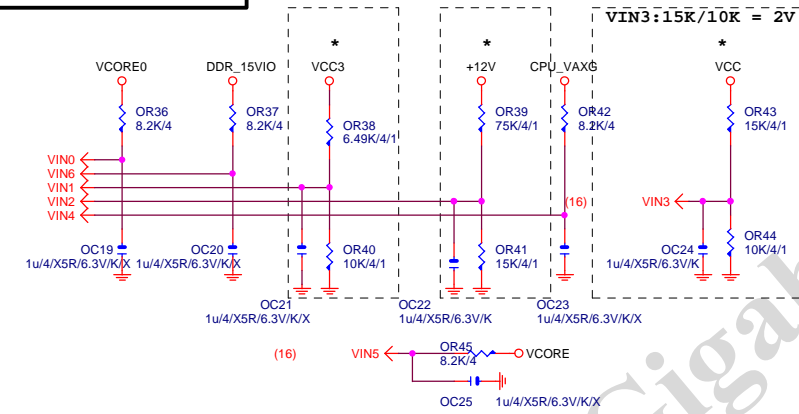
TEMP H/W MONITOR



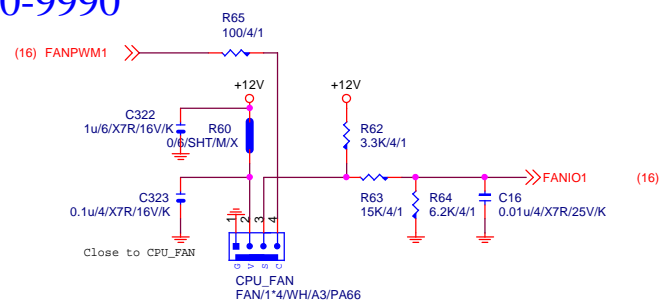
CASE OPEN



VOLTAGE-- H/W MONITOR

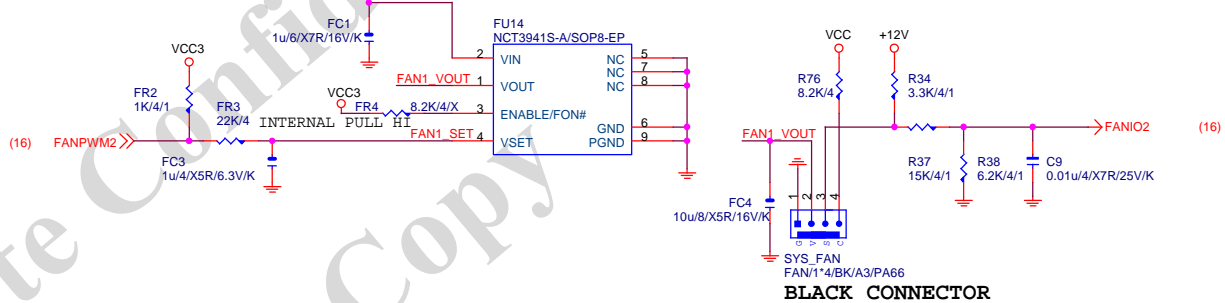


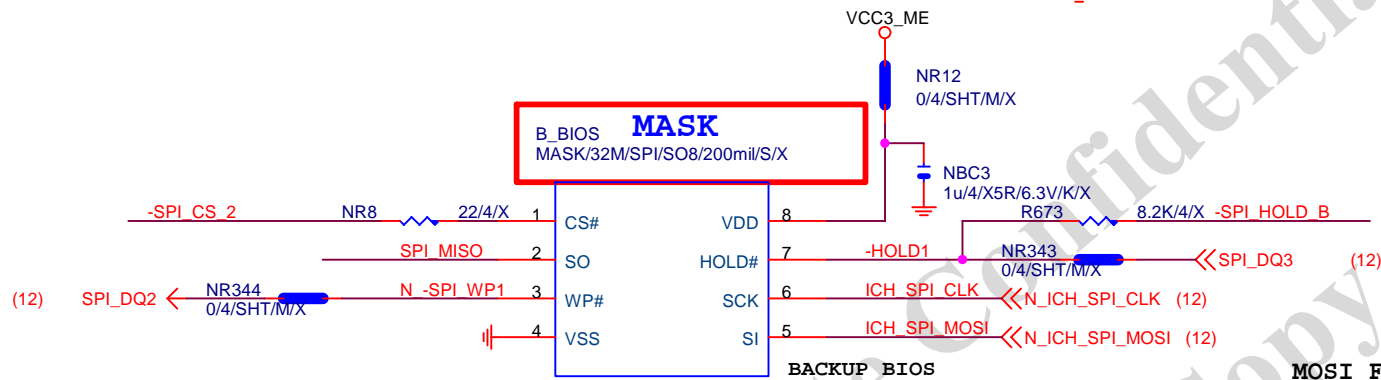
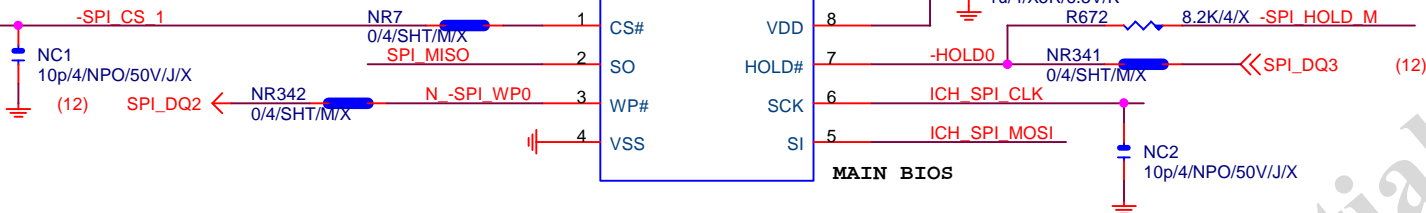
CPU SMART FAN



SYS SMART FAN

Linear SYS_FAN
Enable Function (NCT3941S)
Full Turn On Function (NCT3941S-A)

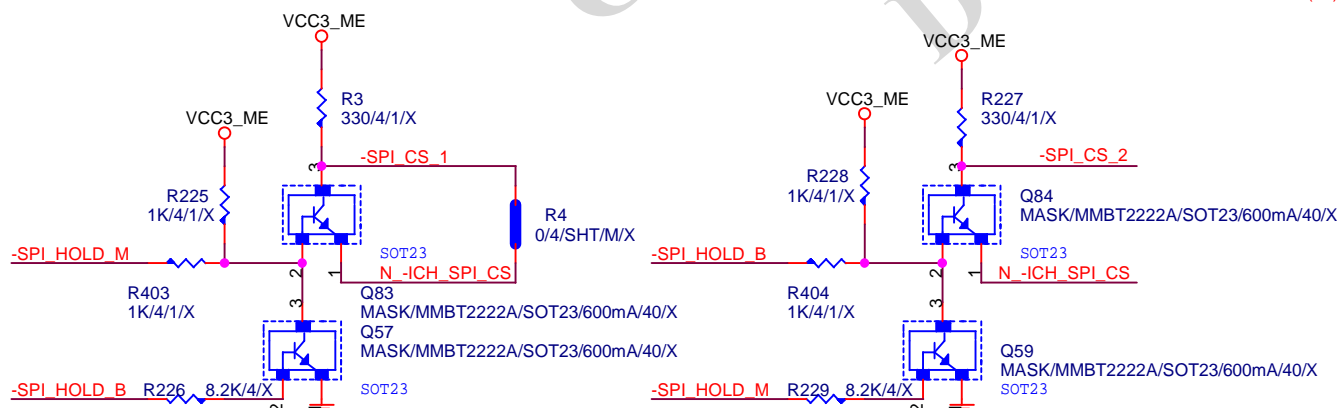
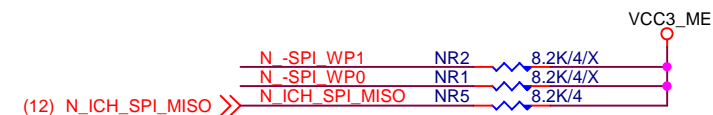
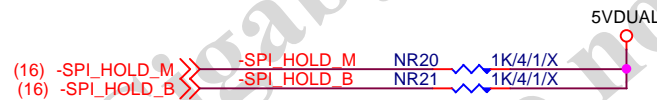
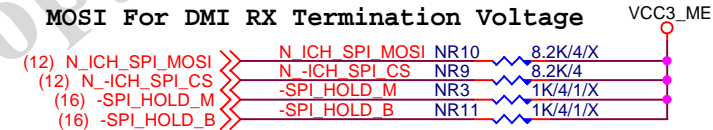




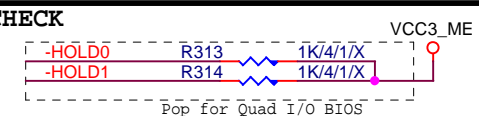
BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

1 means floating
0 means PD 1K

MOSI For DMI RX Termination Voltage



CHECK



Gigabyte Technology

DUAL BIOS

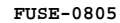
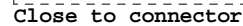
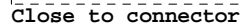
Title	GA-H81M-H		Rev 2.1
Size Custom	Document Number		
Date	Thursday, November 20, 2014	Sheet	19 of 29

Remove Level shift

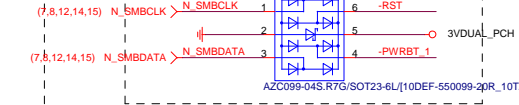
SPKR



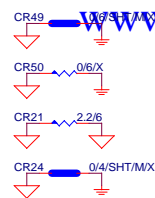
INTEL FRONT PANEL



技術通報 No. 79



Title		FP,F_USB,USB PWR,SPKR,SATA LED	
Doc No: 9001-103	Document Number	GA-H81M-H	Rev 2.1
Date:	Thursday, November 20, 2014	Sheet	20 of 29

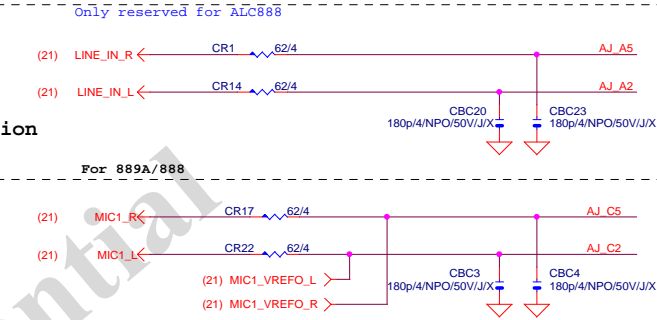


www.xinxunwei.com 400-800-9990

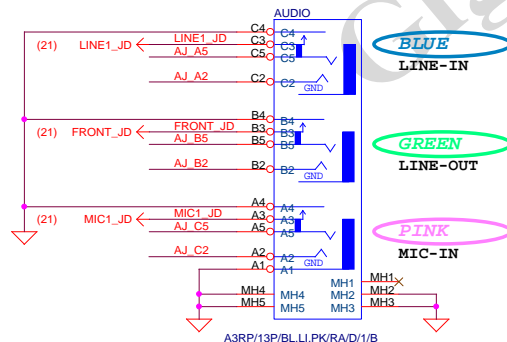
LINE-IN

Verify MIC function
in LINE-in

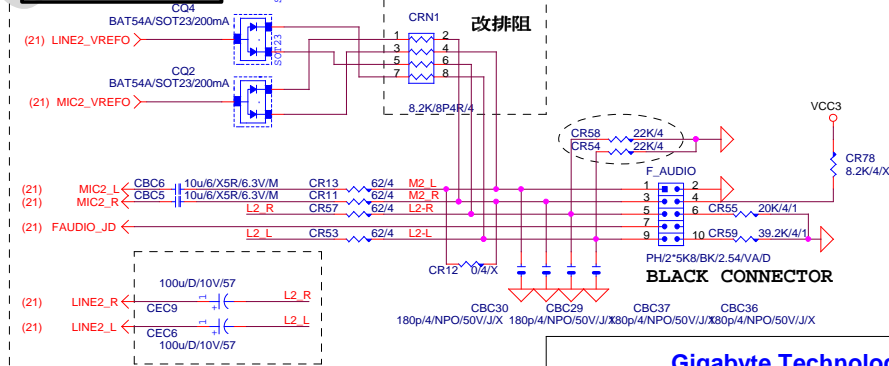
MIC-IN



SPDIF_OUT



AZALIA FRONT PANEL



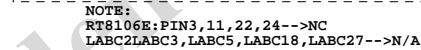
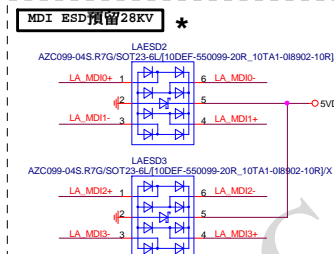
Gigabyte Technology

AUDIO JACK

GA-H81M-H

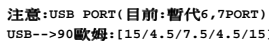
Rev 2.1

Date: Thursday, November 20, 2014 Sheet 22 of 29



料號	規格	廠商
11NR6-702009-96R	1G LAN (12core)	UDE(RU9 ESD+)
[LED獨立走線,可省略外加AZC099料件LAESD1]		

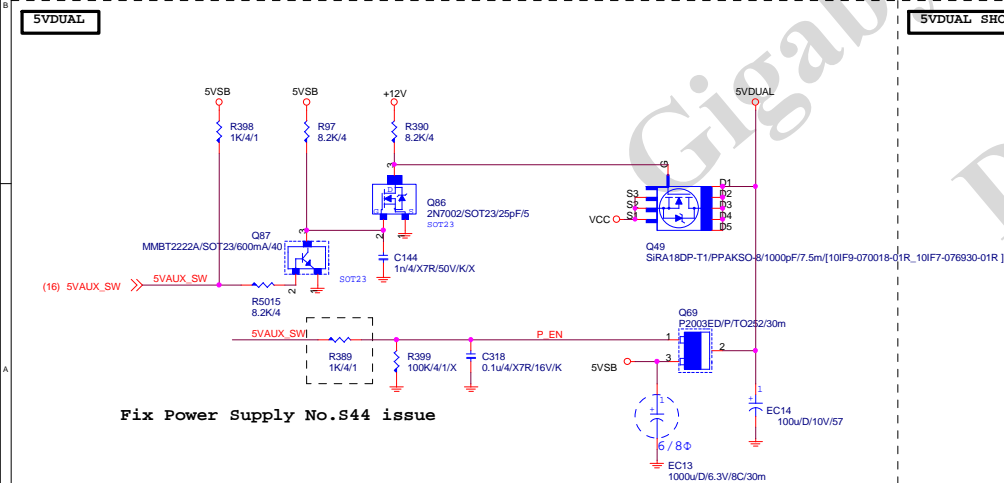
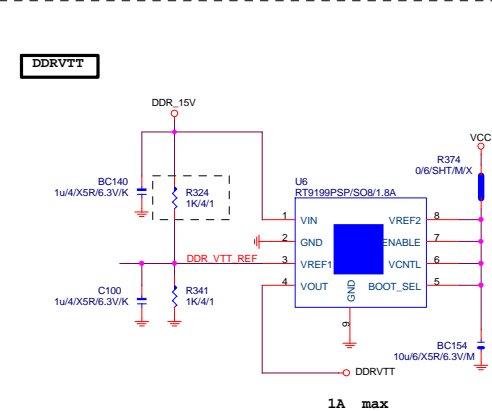
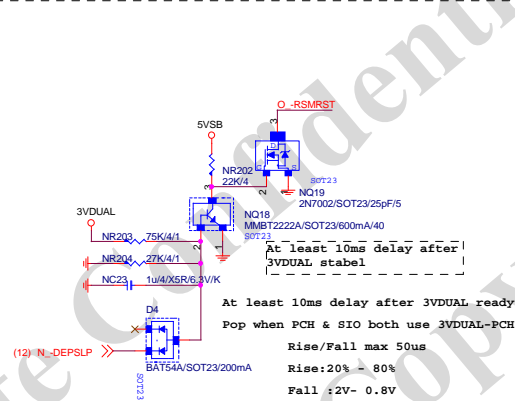
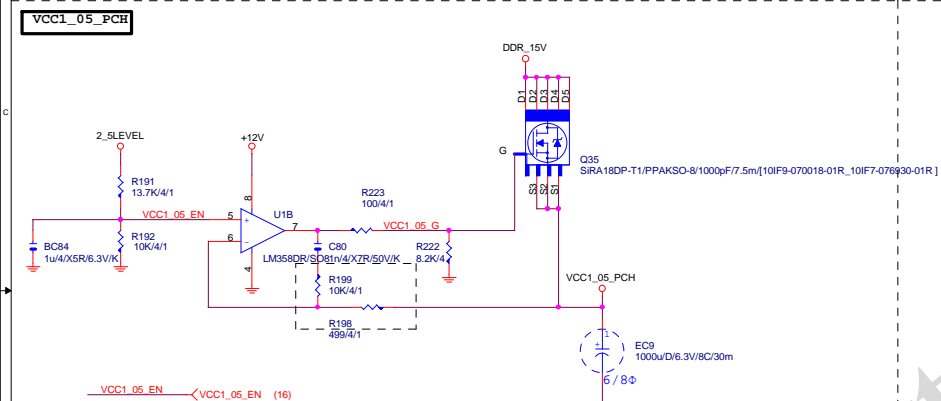
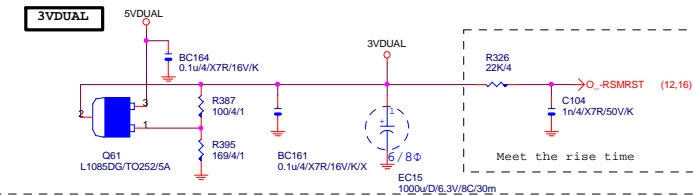
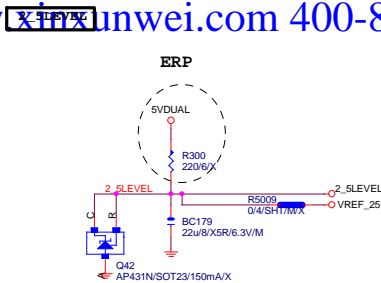
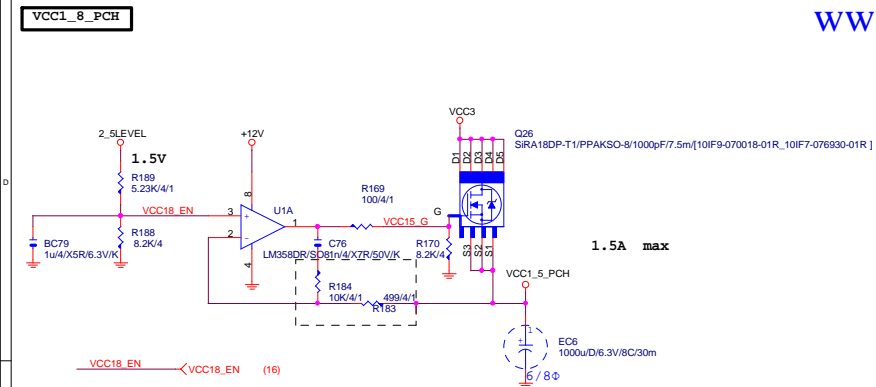
1. 9KV ESD BOM:
USB_LAN (RU9):11NR6-702009-96R
2. 28KV ESD BOM:
USB_LAN (RU9):11NR6-702009-96R
LAESD2, LAESD3: 上件AZC398-04S



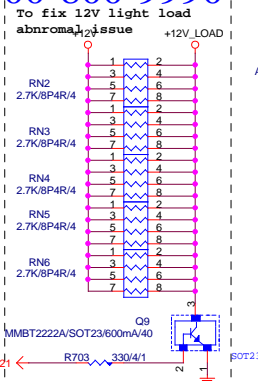
料號	規格	廠商
11NR6-702009-96R 1G LAN (12core)		UDE(RU9 ESD+)
[LED獨立走線,可省略外加AZC099料件LAESD1]		

1. 9KV ESD BOM:
USB_LAN (RU9):11NR6-702009-96R
2. 28KV ESD BOM:
USB_LAN (RU9):11NR6-702009-96R
LAESD2, LAESD3: 上件AZC398-04S

Gigabyte Technology			
Title			
Realtek RTL8111G			
Size Custom	Document Number	GA-H81M-H	Rev 2.1
Date:	Thursday, November 20, 2014	Sheet	23 of 29

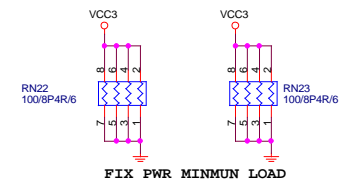


To fix 12V light load
abnromal issue +12V LOAD



To prevent the 5VSB
under loading when
boot

【技術通報R&D技術通報154】

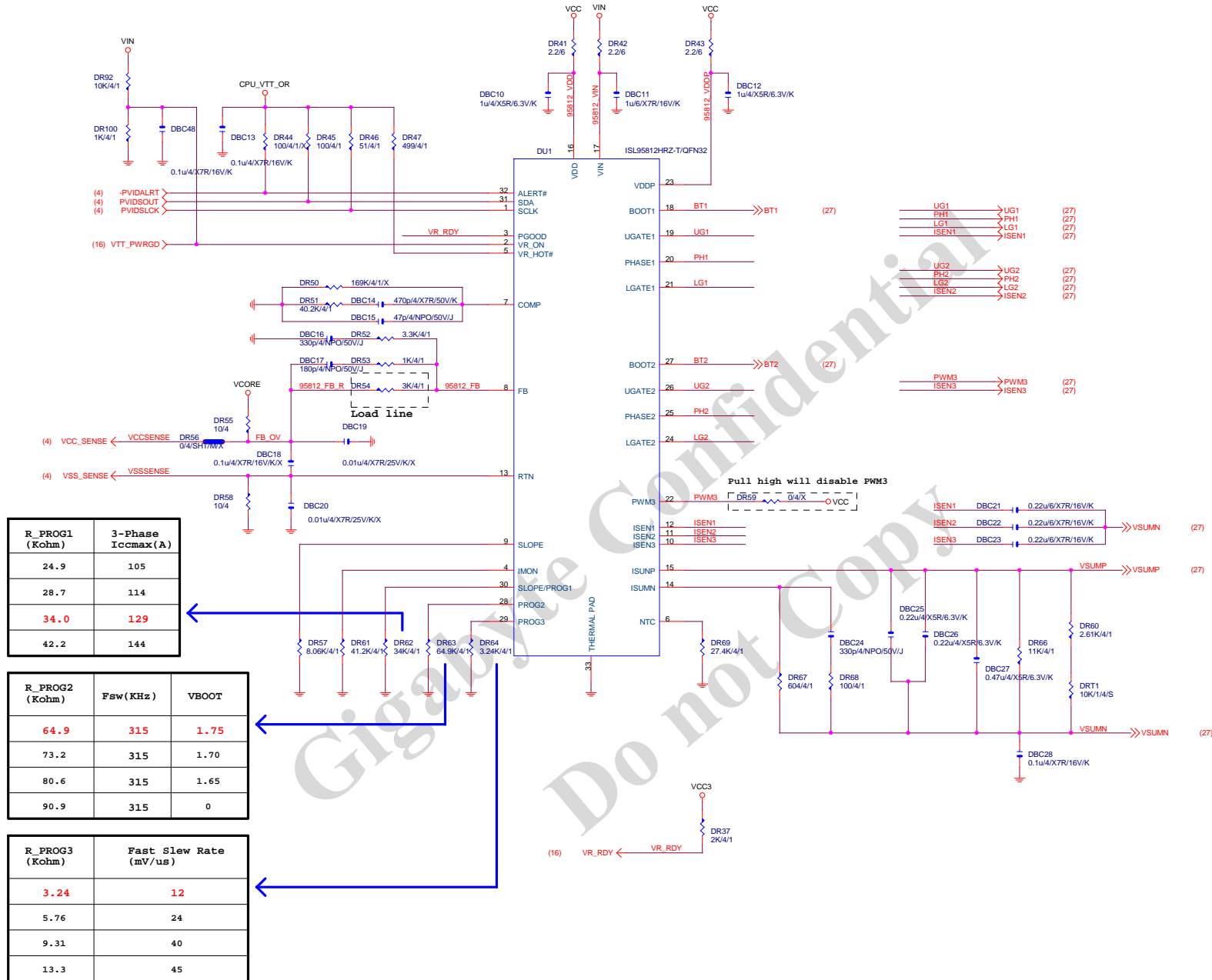


Gigabyte Technology

ATX CONNECTOR

GA-H81M-H

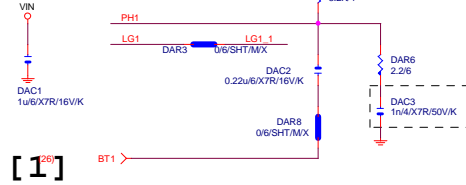
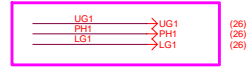
Rev	2.1
-----	-----



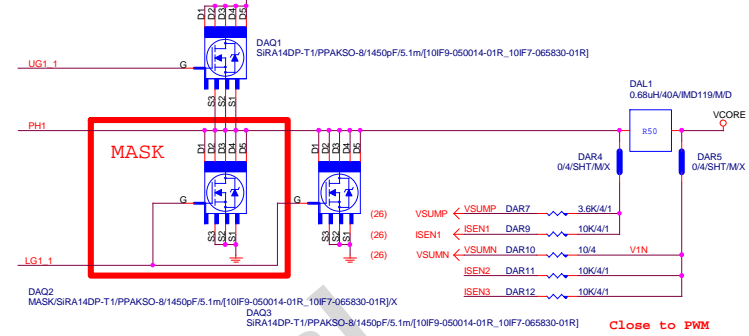
Gigabyte Technology

File		
CPU CORE VR-1		
Size	Document Number	Rev
Custom	GA-H81M-H	2.1
Date	Thursday, November 20, 2014	Sheet 26 of 29

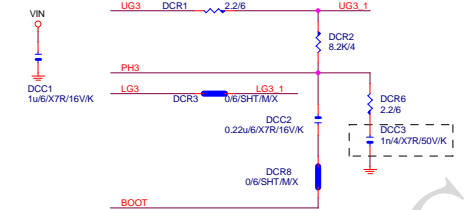
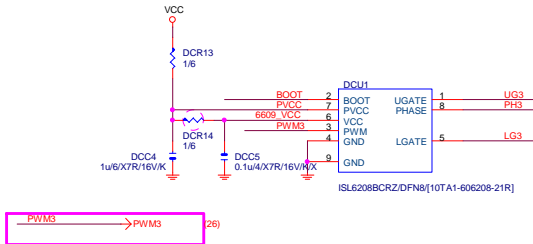
PHASE 1



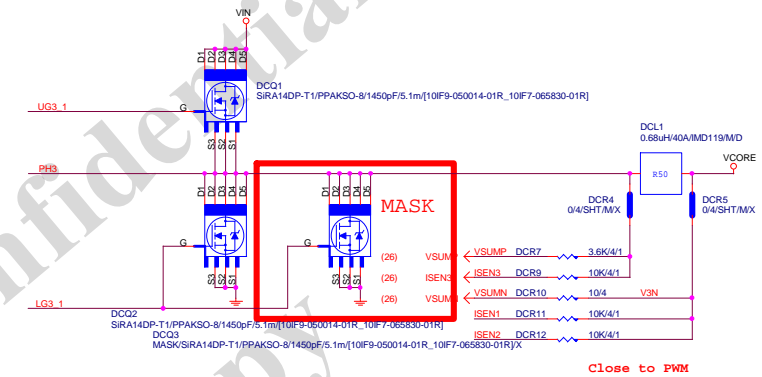
[1]



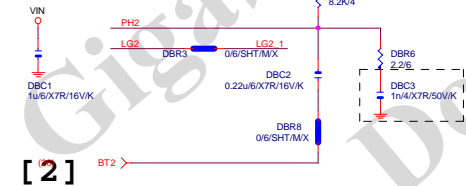
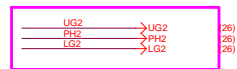
PHASE 3



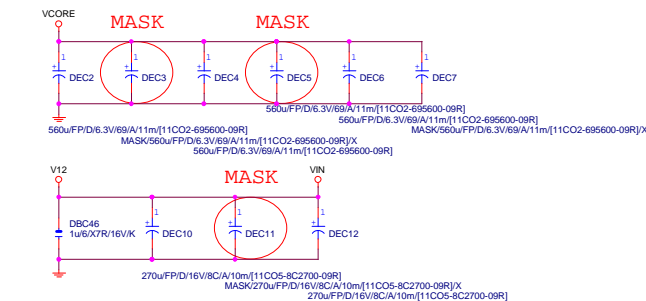
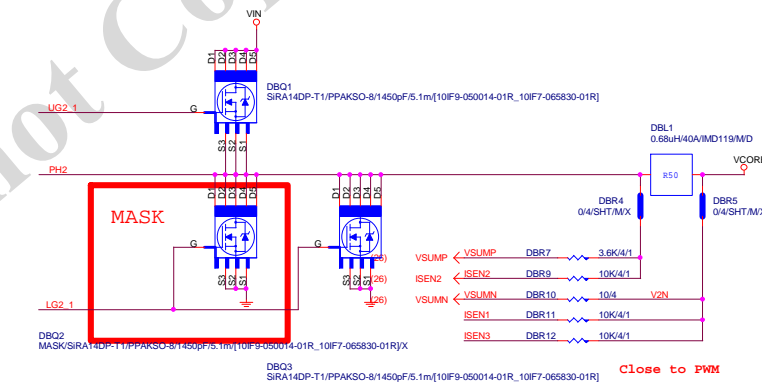
[3]



PHASE 2

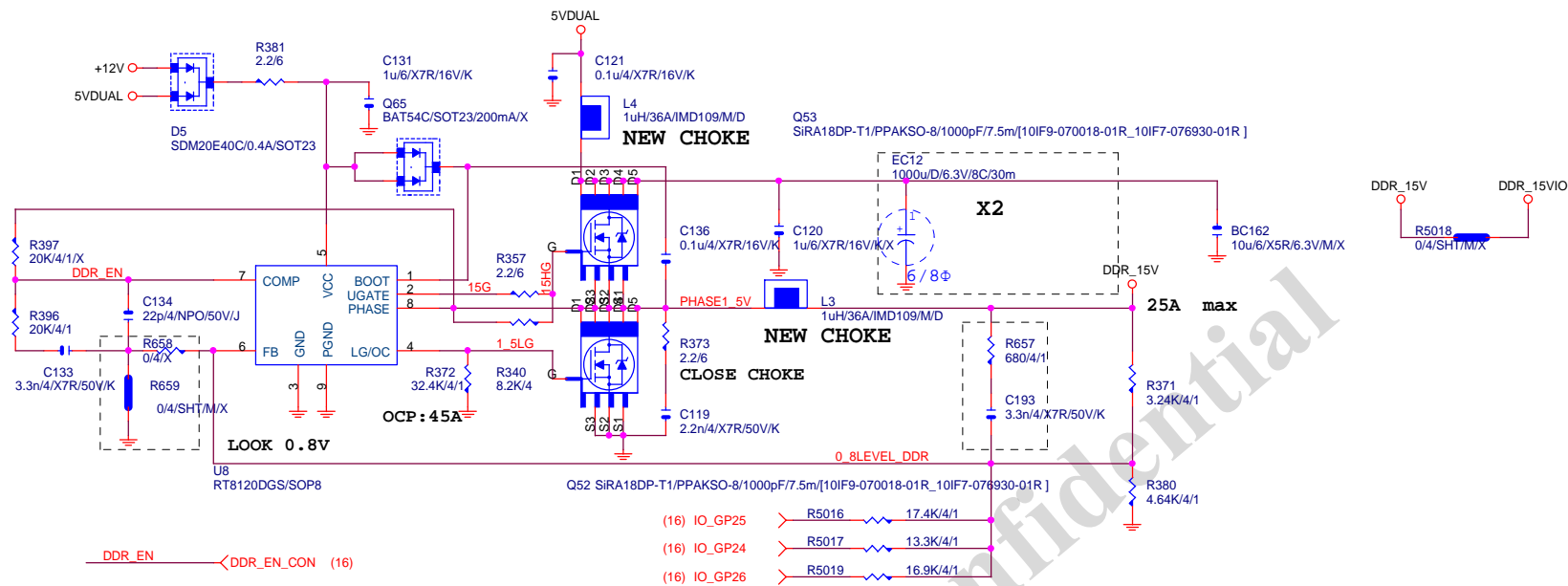


[2]



Gigabyte Technology

Title		CPU CORE VR-2	
Size	Document Number	GA-H81M-H	Rev
Custom			2.1
Date:	Thursday, November 20, 2014	Sheet	27 of 29



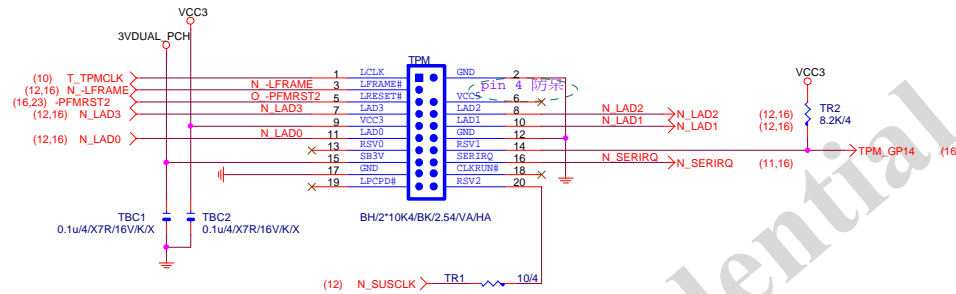
VIN=5V,VOUT=1.5V,IOUT=25A,PHASE=1
IRMS=11.45A
560uF/P/D/6.3V/68/8m RIPPLE CURRENT=4.7A
Coefficient=1.7(85°C),1(105°C)

VIN Ripple current=4.7X1.7=7.99A(85°C)
-->故固態電容須2X7.99=15.98>11.45A

$$\begin{aligned} \text{Rocset} &= (\text{Iocp} * \text{Lgate}, \text{rdson}) / \text{Iocset} \\ \text{Rocset} &= (45\text{A} * 6.7\text{mOhm}) / 10\text{uA} = 30\text{K} \\ \text{Iocset} &= 10\text{uA} \end{aligned}$$

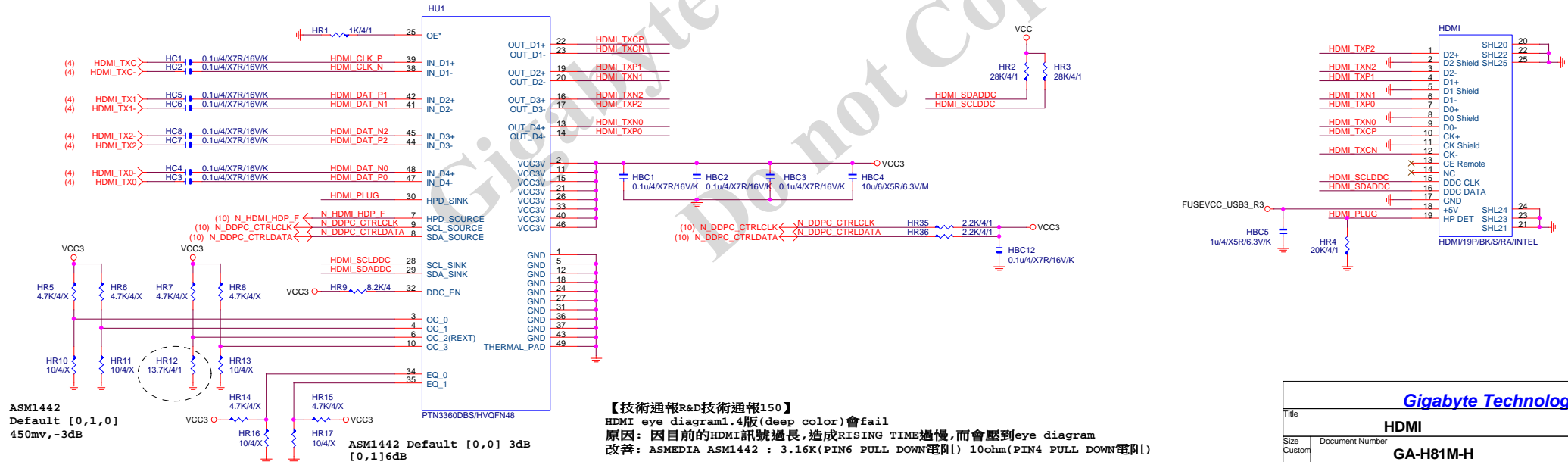
<i>Gigabyte Technology</i>			
Title			
DDR POWER			
Size	Document Number	GA-H81M-H	Rev
Custom			2.1
Date:	Thursday, November 20, 2014	Sheet	28 of 29

TPM CONNECT



HDMI LEVEL SHIFT

HDMI: 20/4/6/4/20
Impedance=85 +- 17.5%



Gigabyte Technology

HDMI

Size	Document Number	Rev
Custom	GA-H81M-H	2.1
Date:	Thursday, November 20, 2014	Sheet 29 of 29